

THE SINGLE-ENDED S-MATRIX

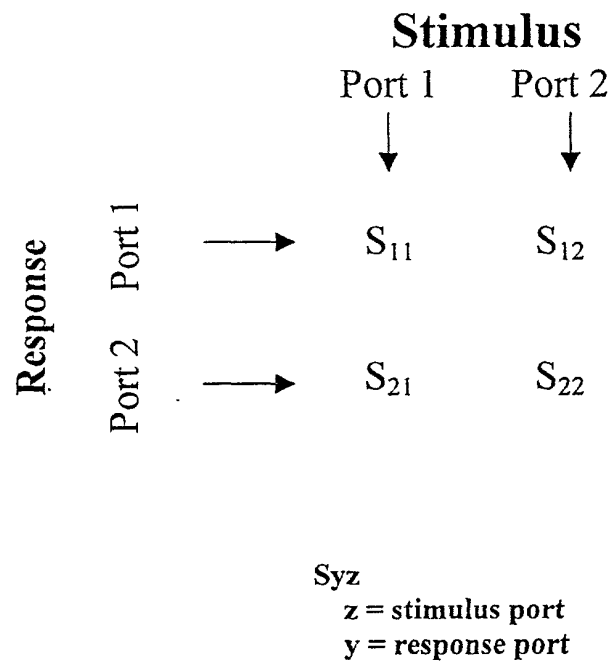


FIG. 1(a)

(Related Art)

THE MIXED-MODE S-MATRIX

		Stimulus			
		Differential Mode		Common Mode	
		Port 1	Port 2	Port 3	Port 4
Response	Differential Mode	Port 1 ↓ → S_{DD11}	Port 2 ↓ → S_{DD12}	Port 3 ↓ → S_{DC11}	Port 4 ↓ → S_{DC12}
	Port 2	→ S_{DD21}	→ S_{DD22}	→ S_{DC21}	→ S_{DC22}
	Common Mode	Port 3 → S_{CD11}	Port 4 → S_{CD12}	→ S_{CC11}	→ S_{CC12}
	Port 4	→ S_{CD21}	→ S_{CD22}	→ S_{CC21}	→ S_{CC22}

S_{wxyz}

w = response mode

z = stimulus port

x = stimulus mode

y = response port

FIG. 1(b)

(Related Art)



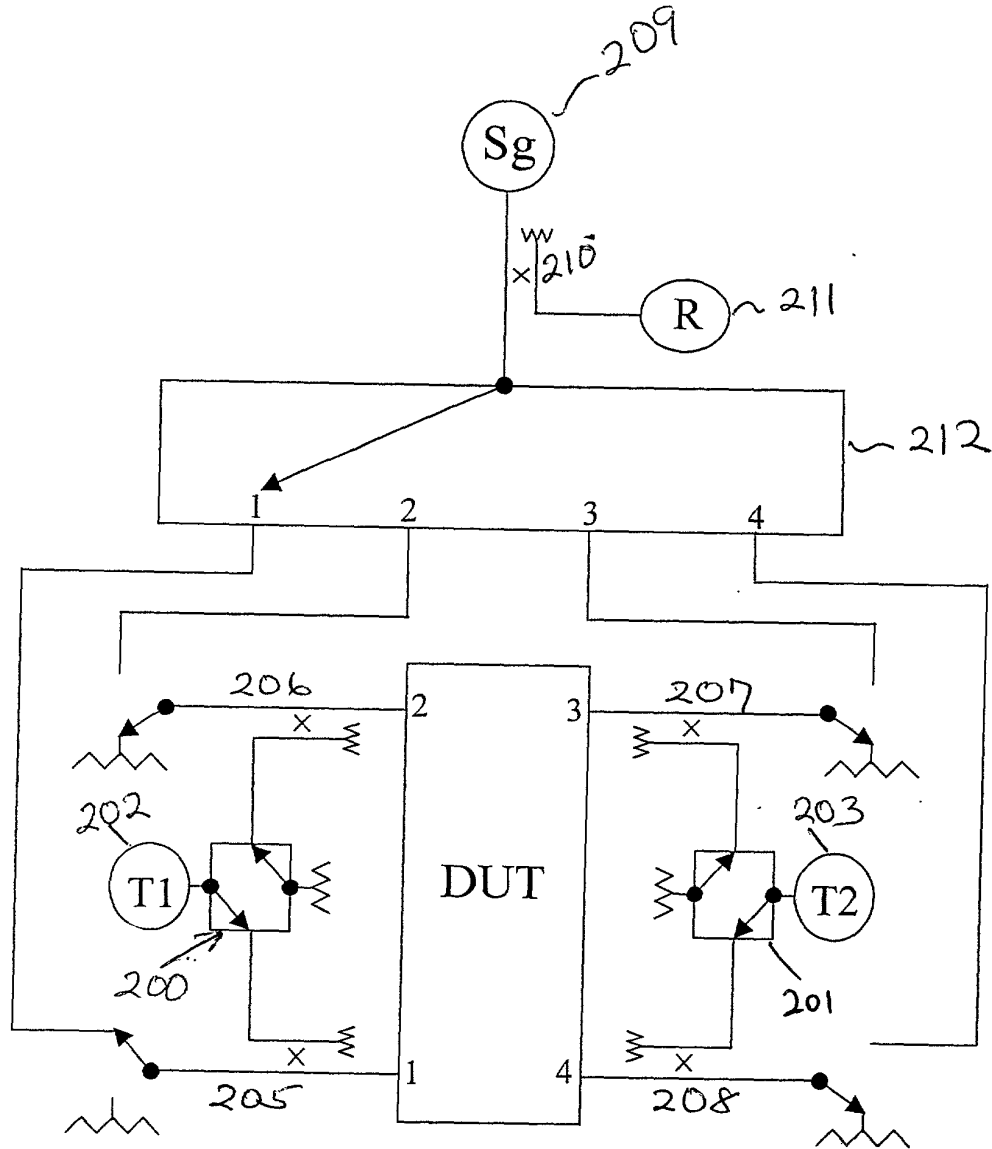


FIGURE 3

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9-Port MTS Using 1 Reference & 3 Test Channel Receiver

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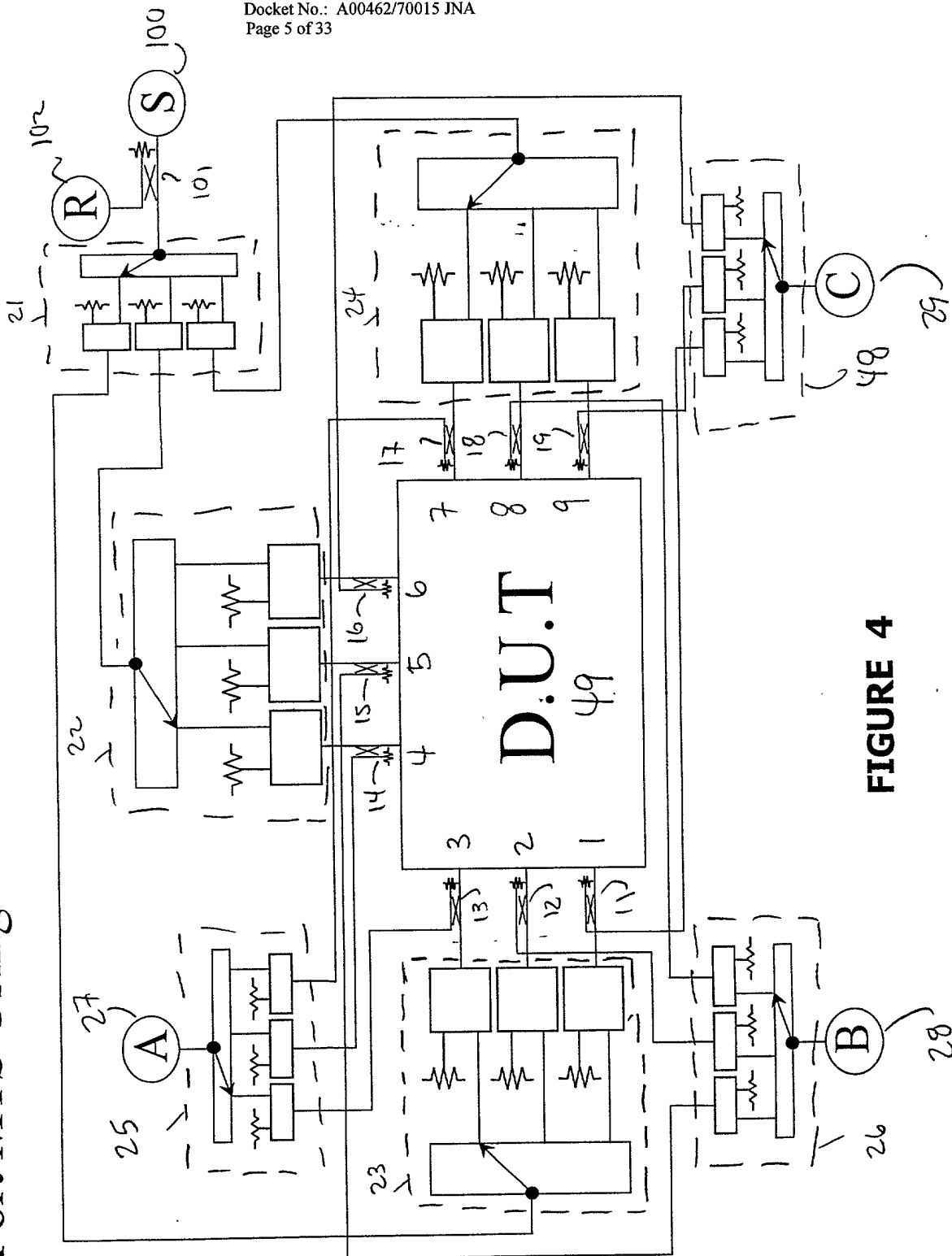


FIGURE 4

Patented 604,660

6-Port MTS Using 1 Reference & 2 Test Channel Receiver

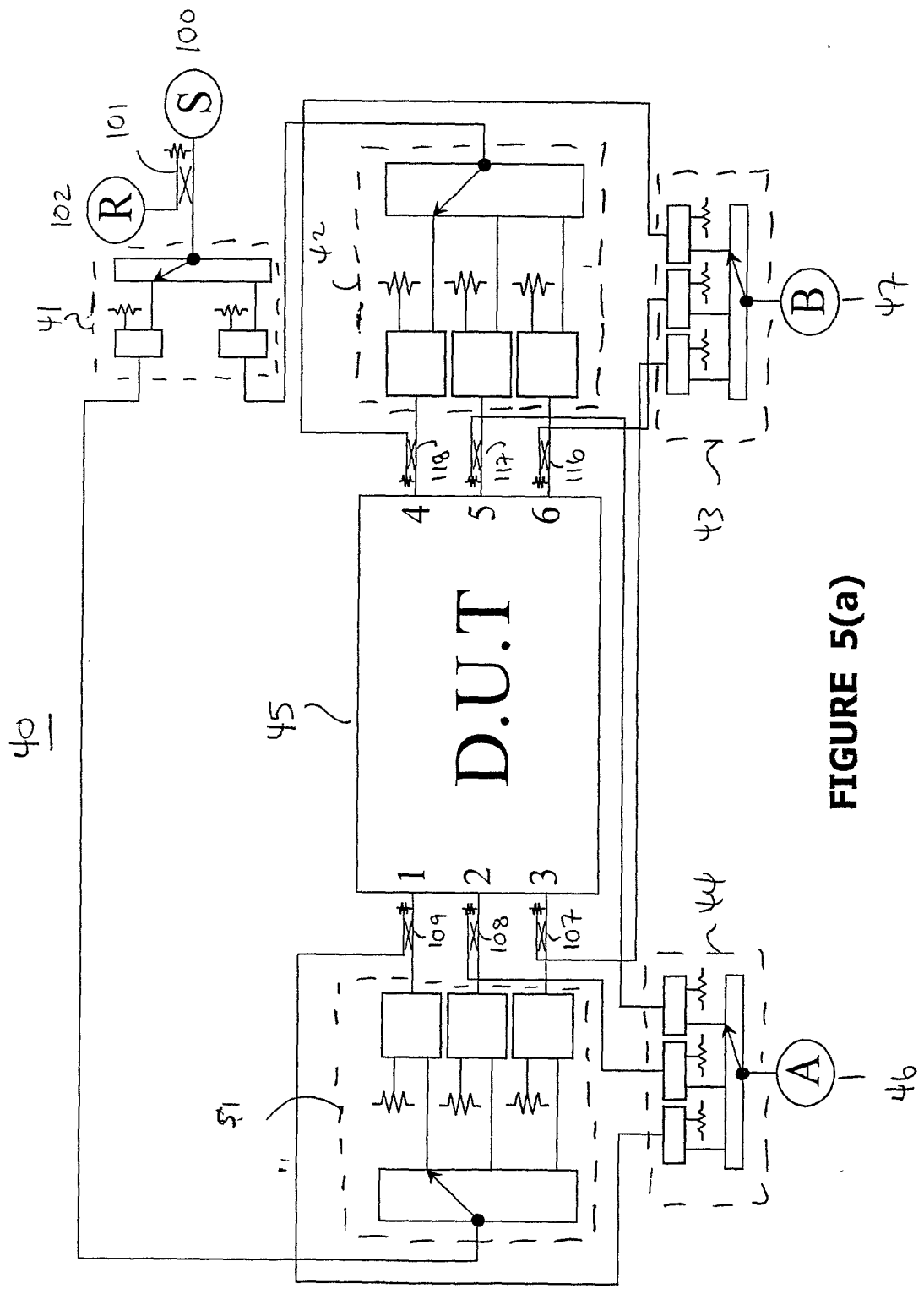


FIGURE 5(a)

6-Port MTS Using 1 Reference & 3 Test Channel Receiver

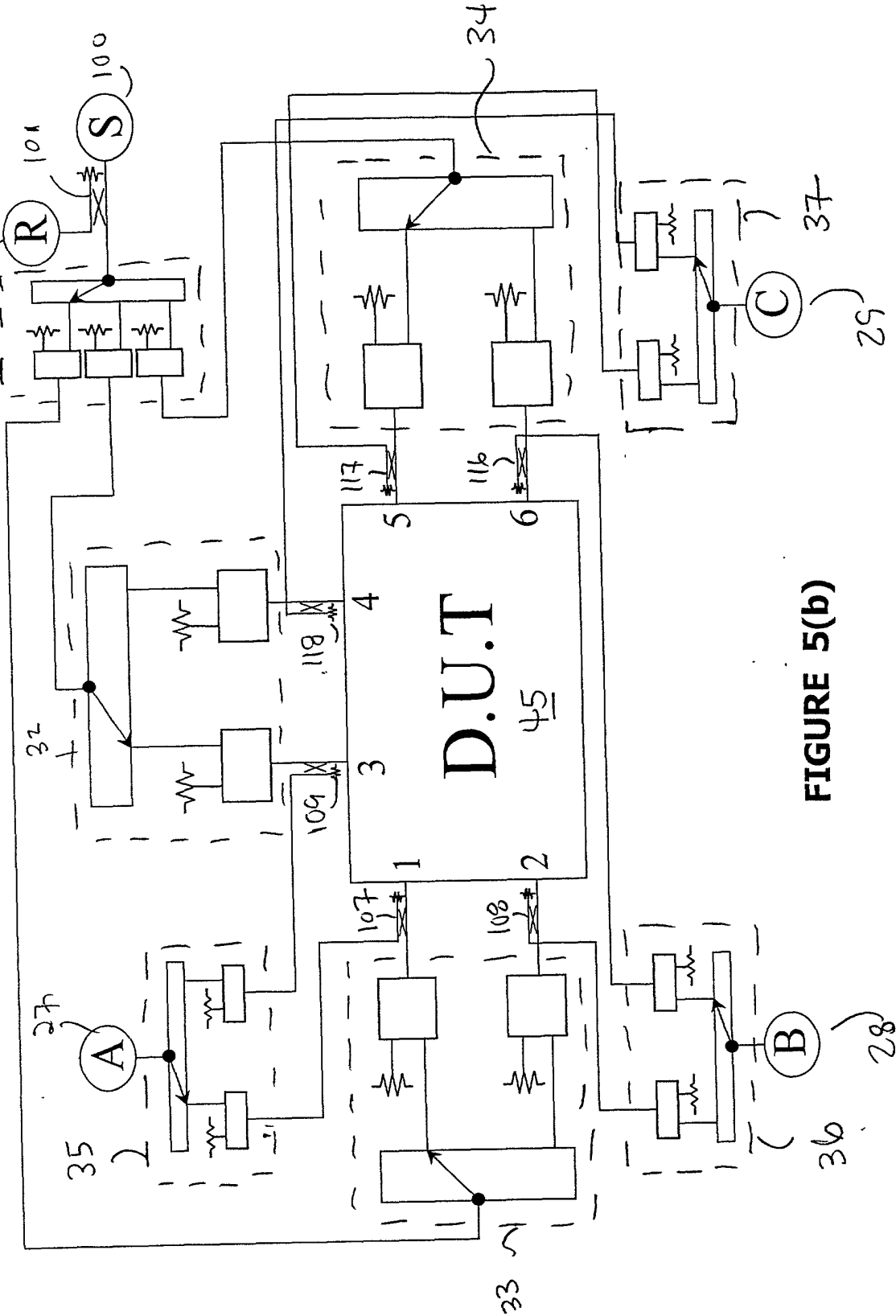


FIGURE 5(b)

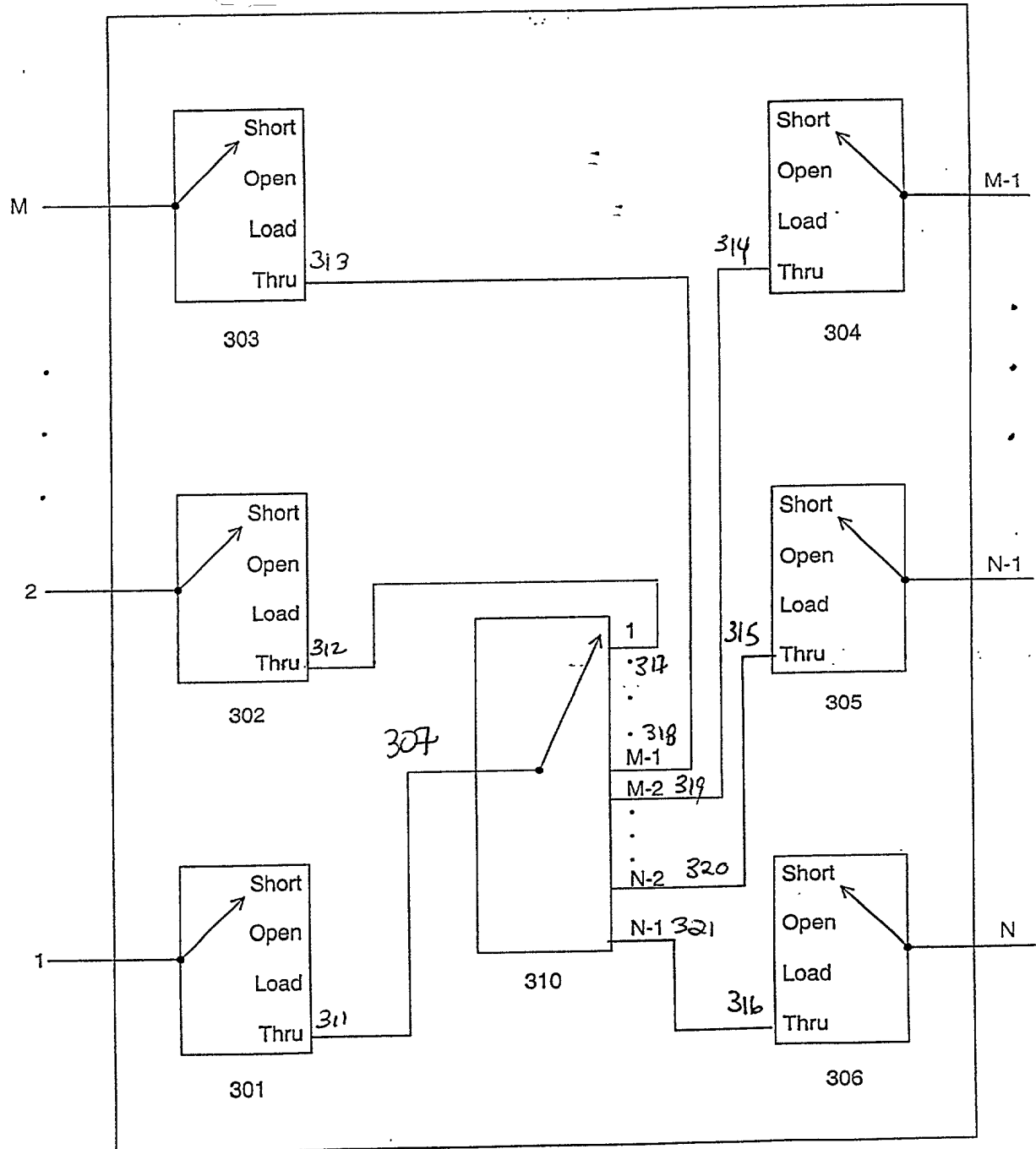


FIGURE 6
(Related Art)

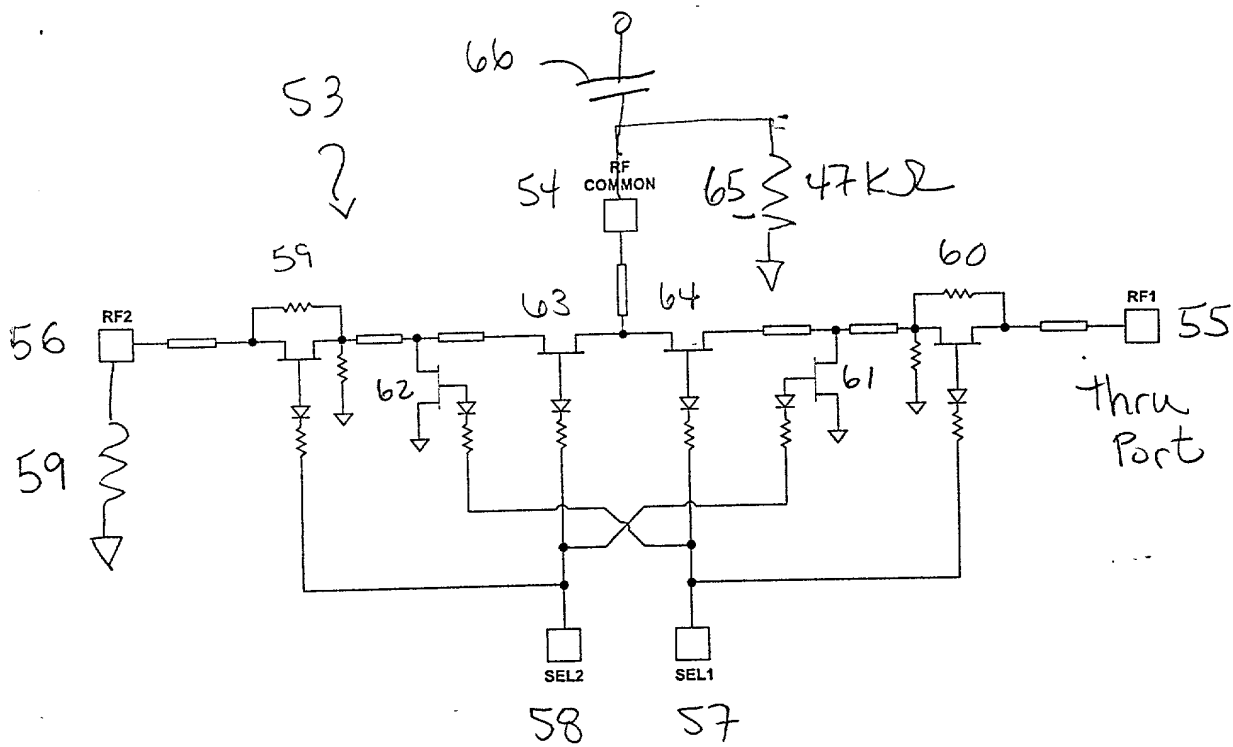


FIGURE 7

FET Switch Configurations

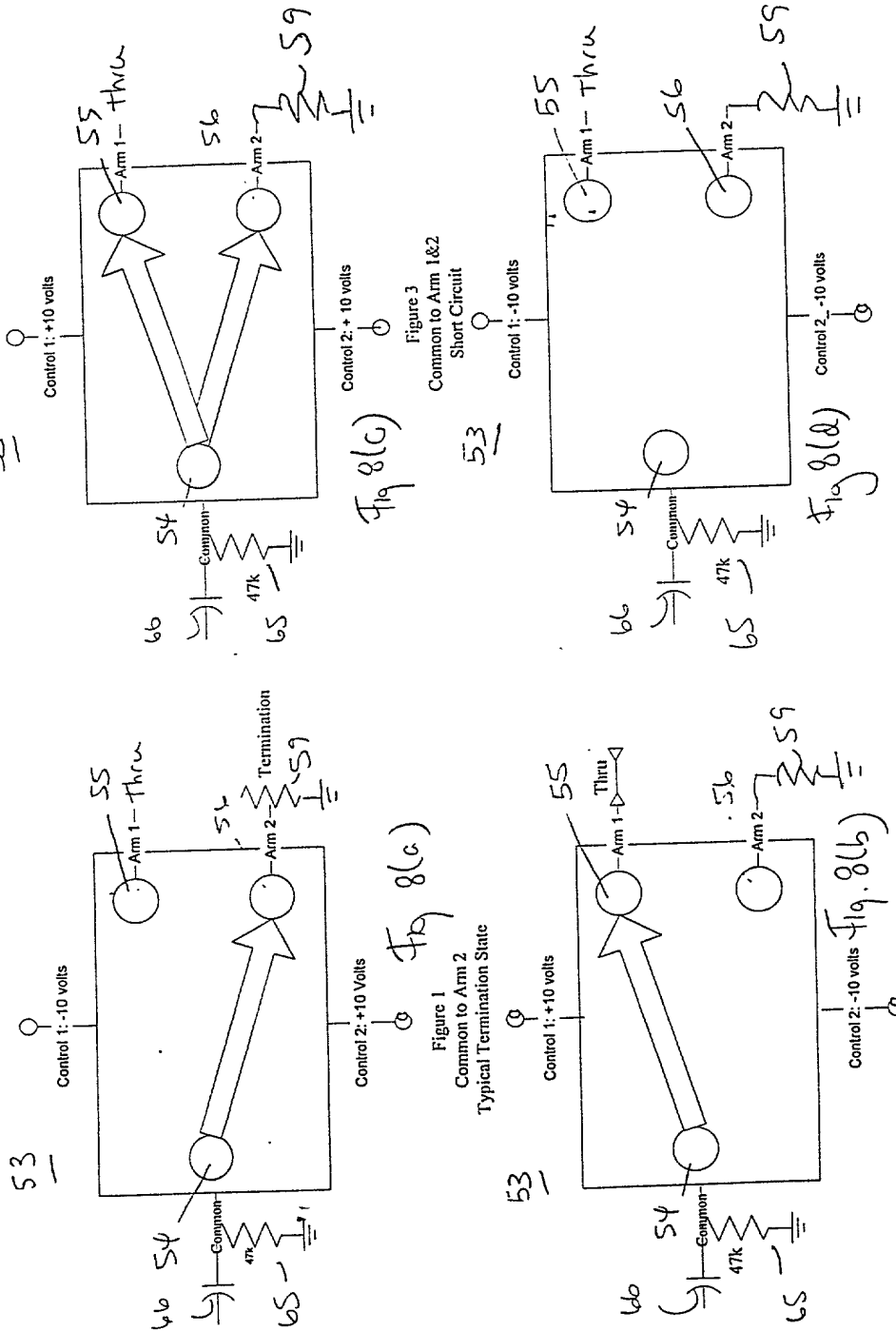


FIGURE 8

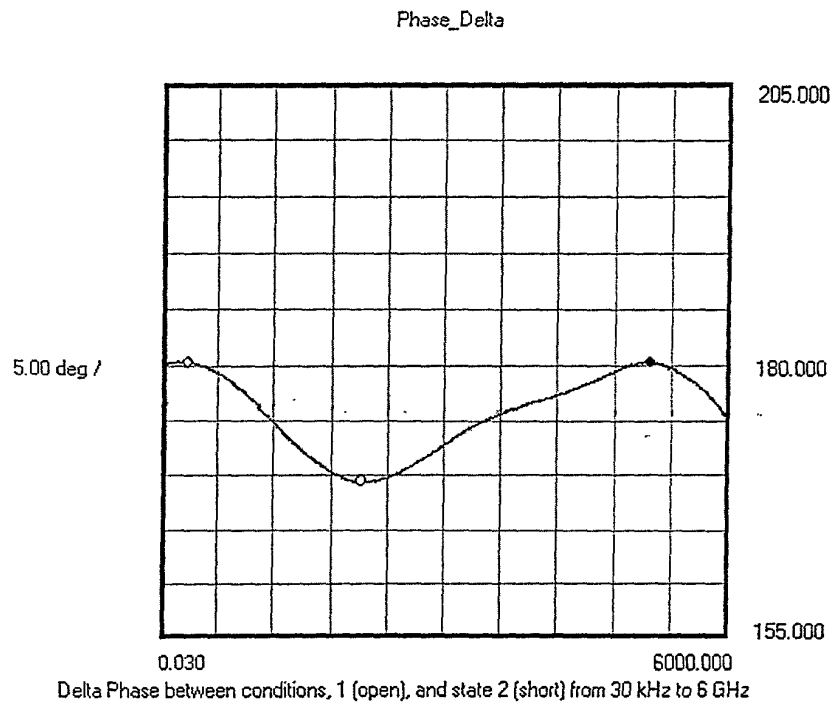


FIGURE 9

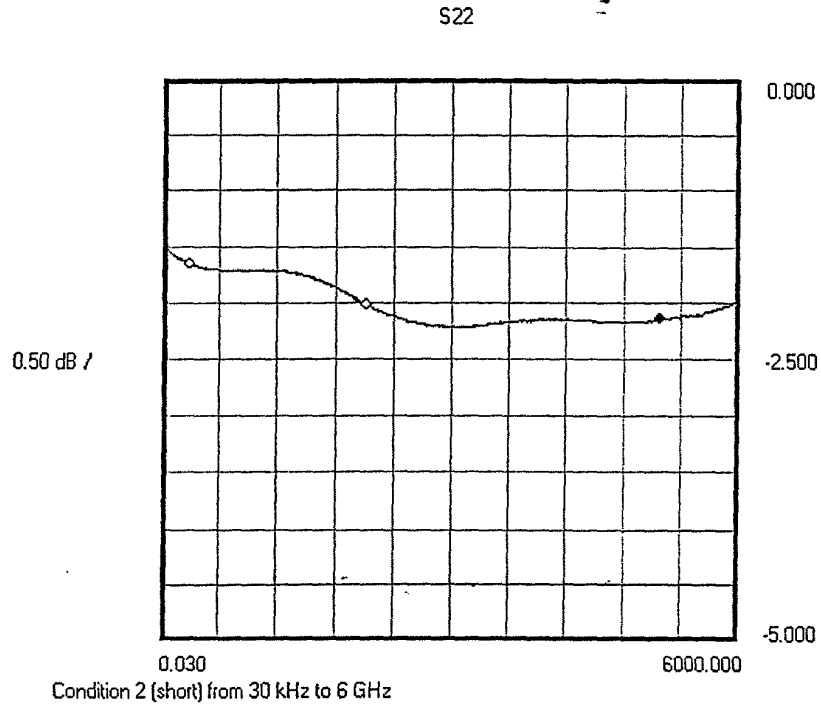


FIGURE 10

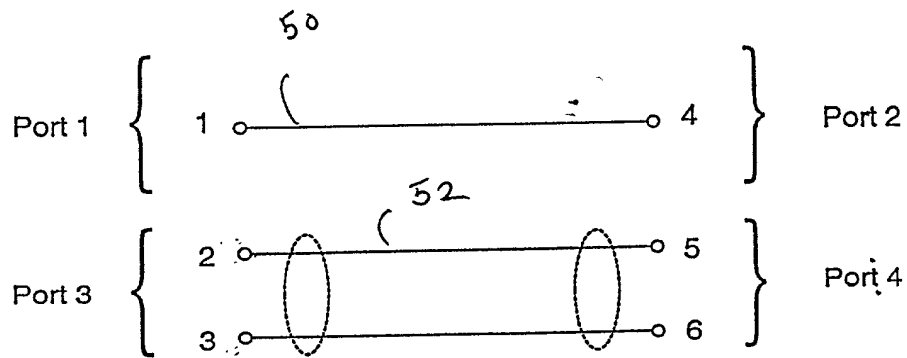


FIGURE 11

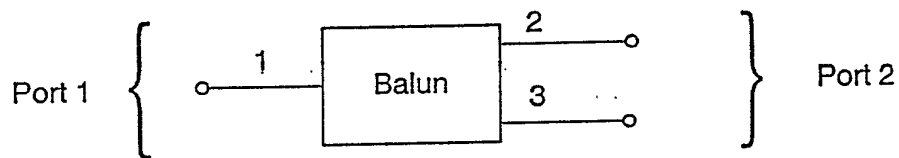


FIGURE 13

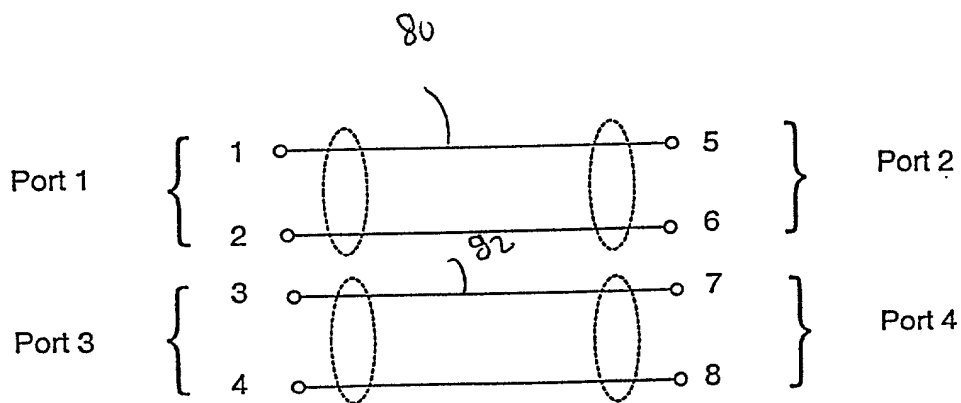


FIGURE 14

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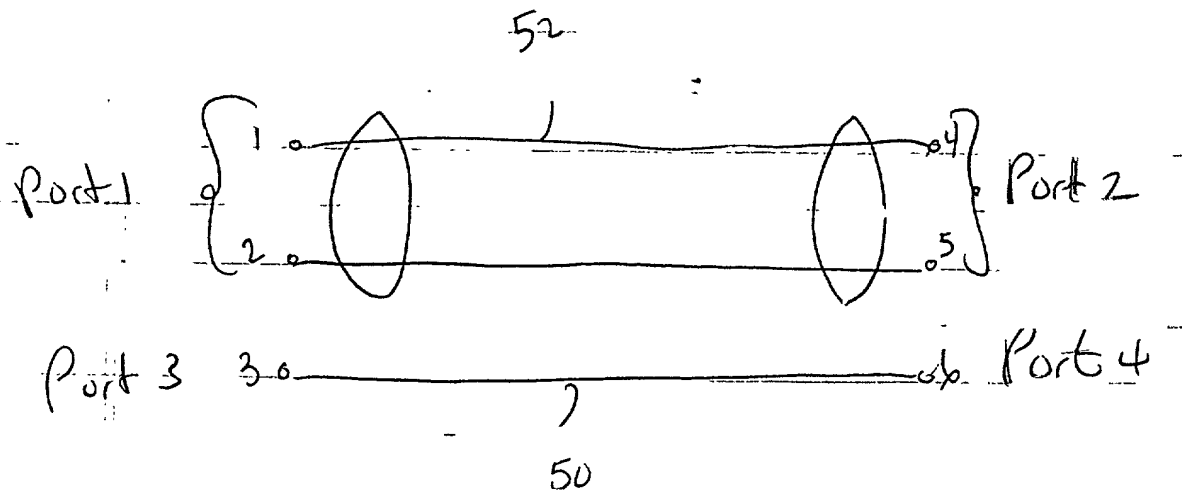


FIGURE 12

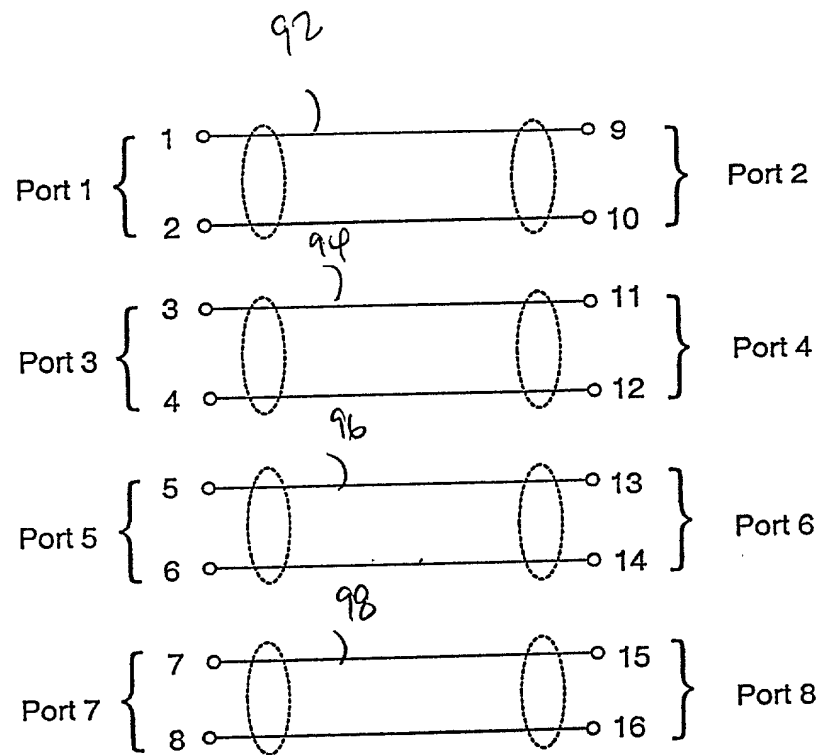


FIGURE 15

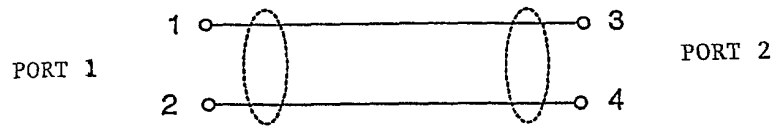


FIGURE 16

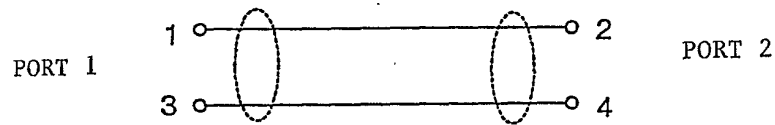


FIGURE 17



FIGURE 18

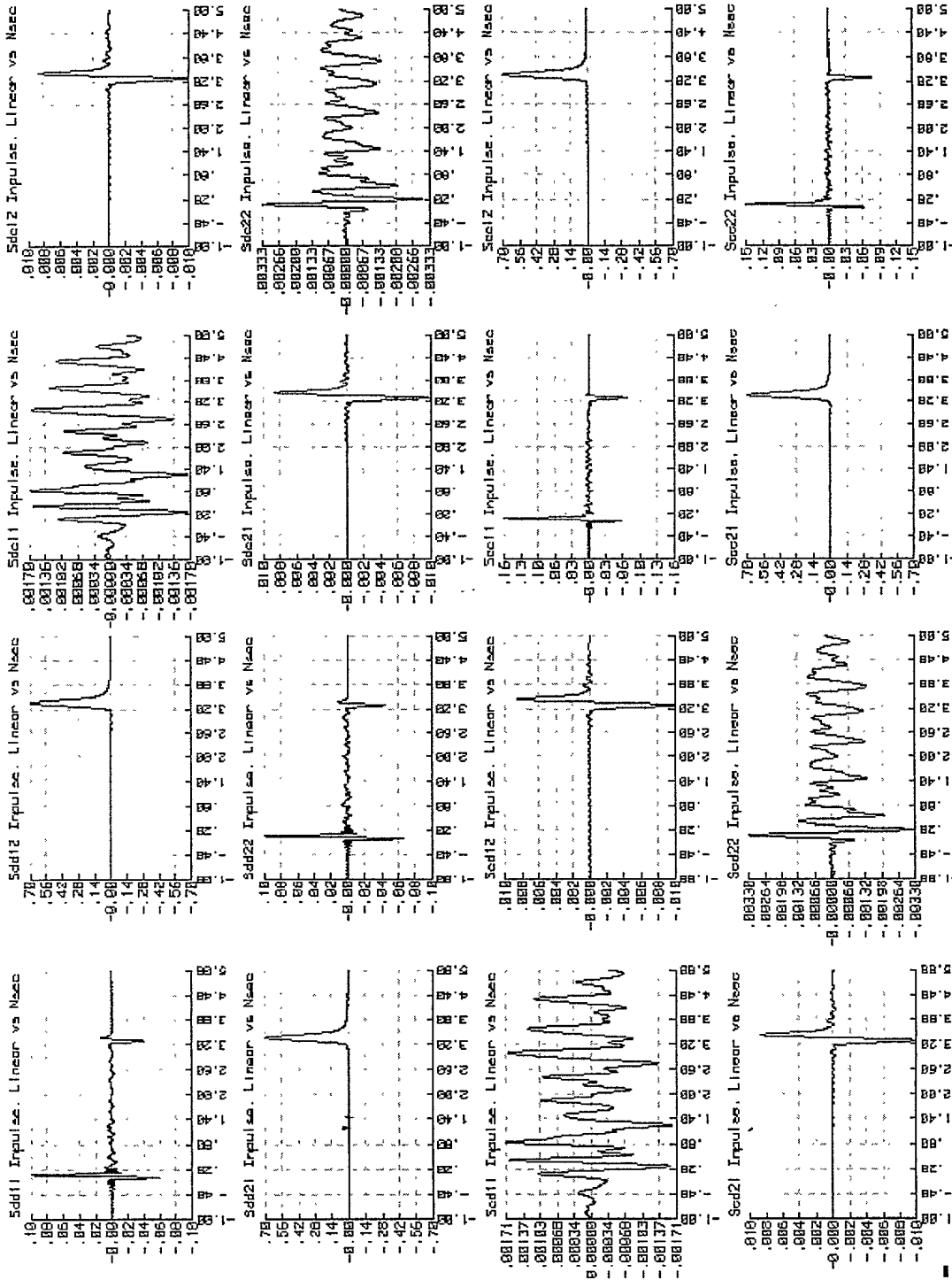


FIGURE 19

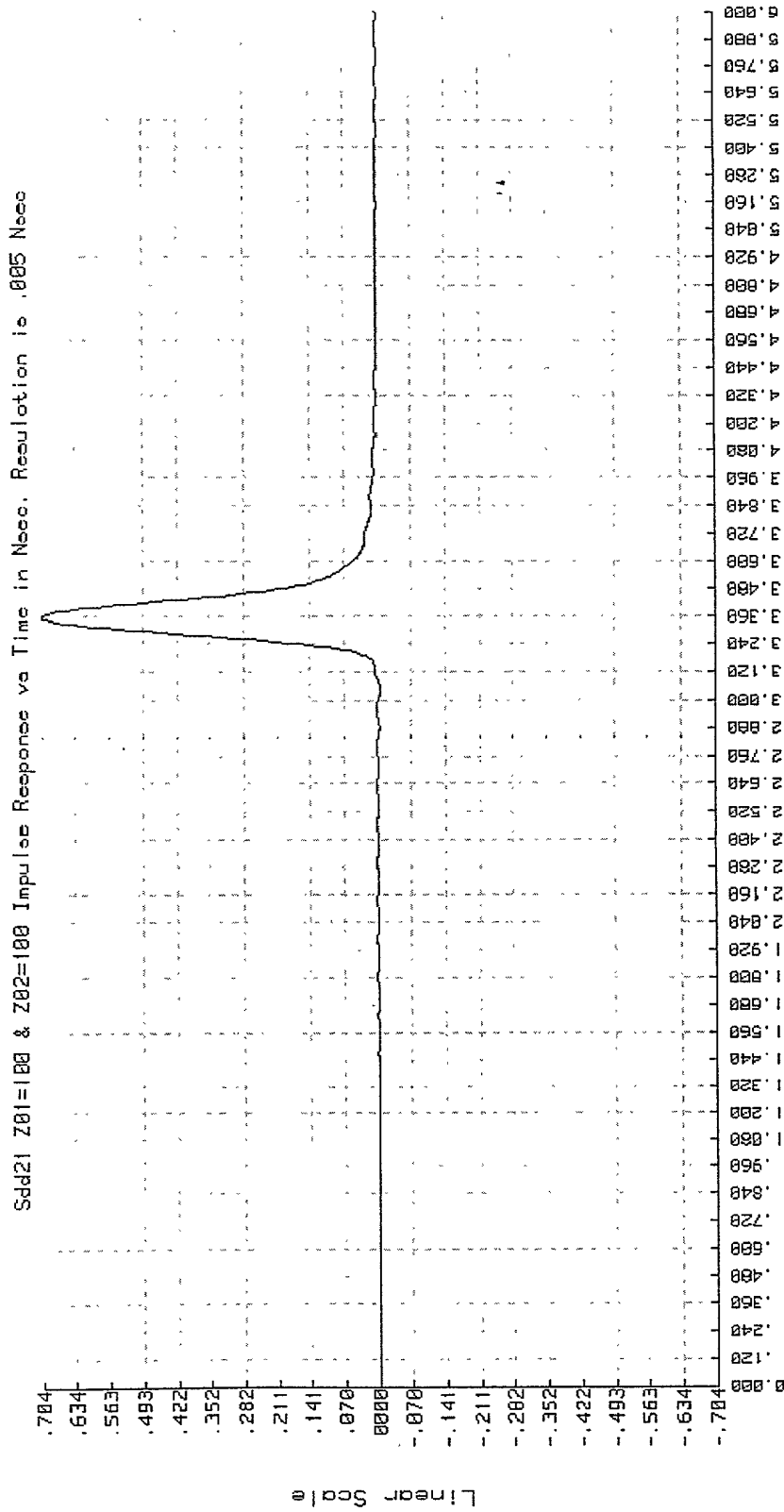


FIGURE 20

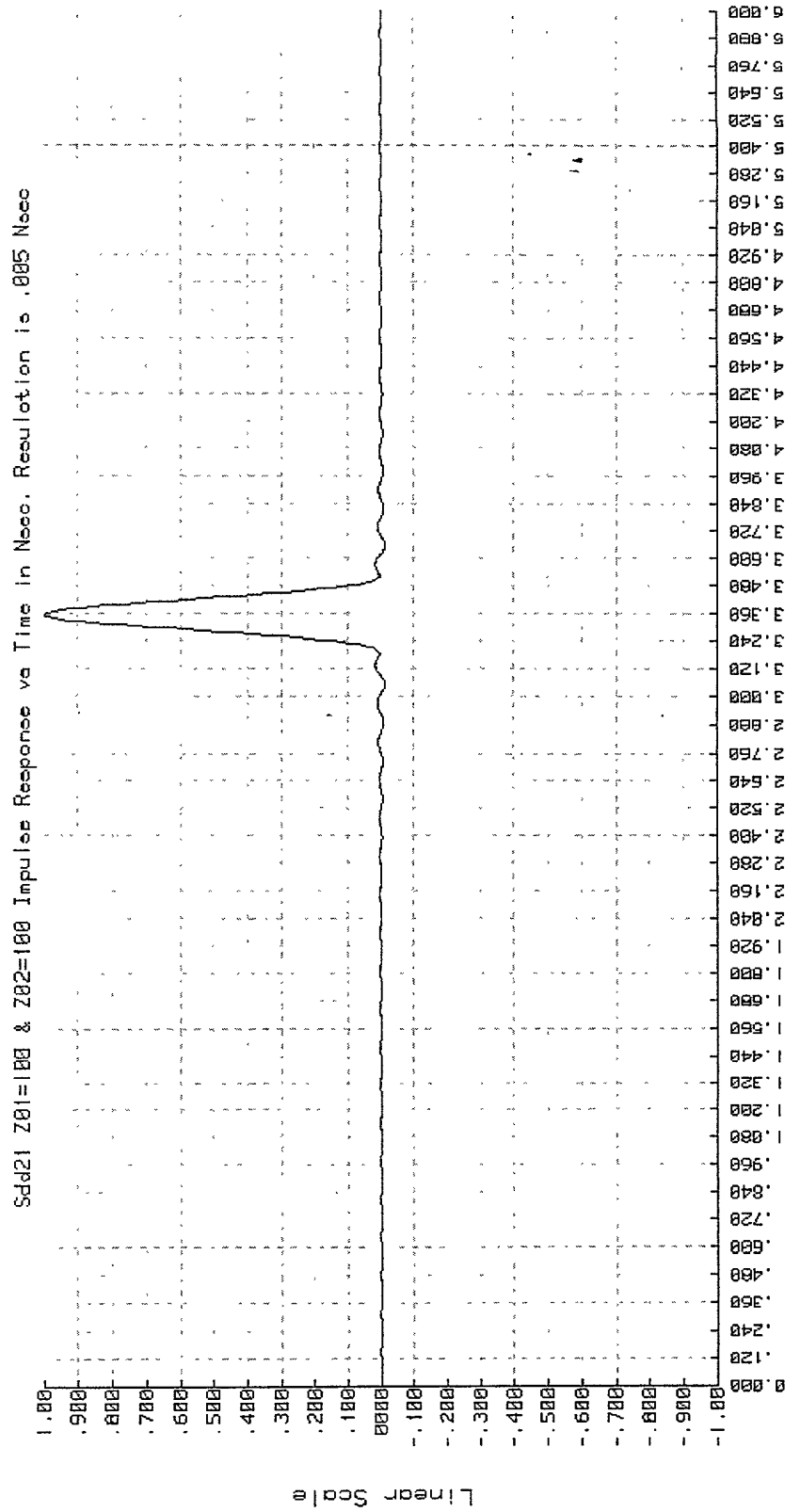


FIGURE 21

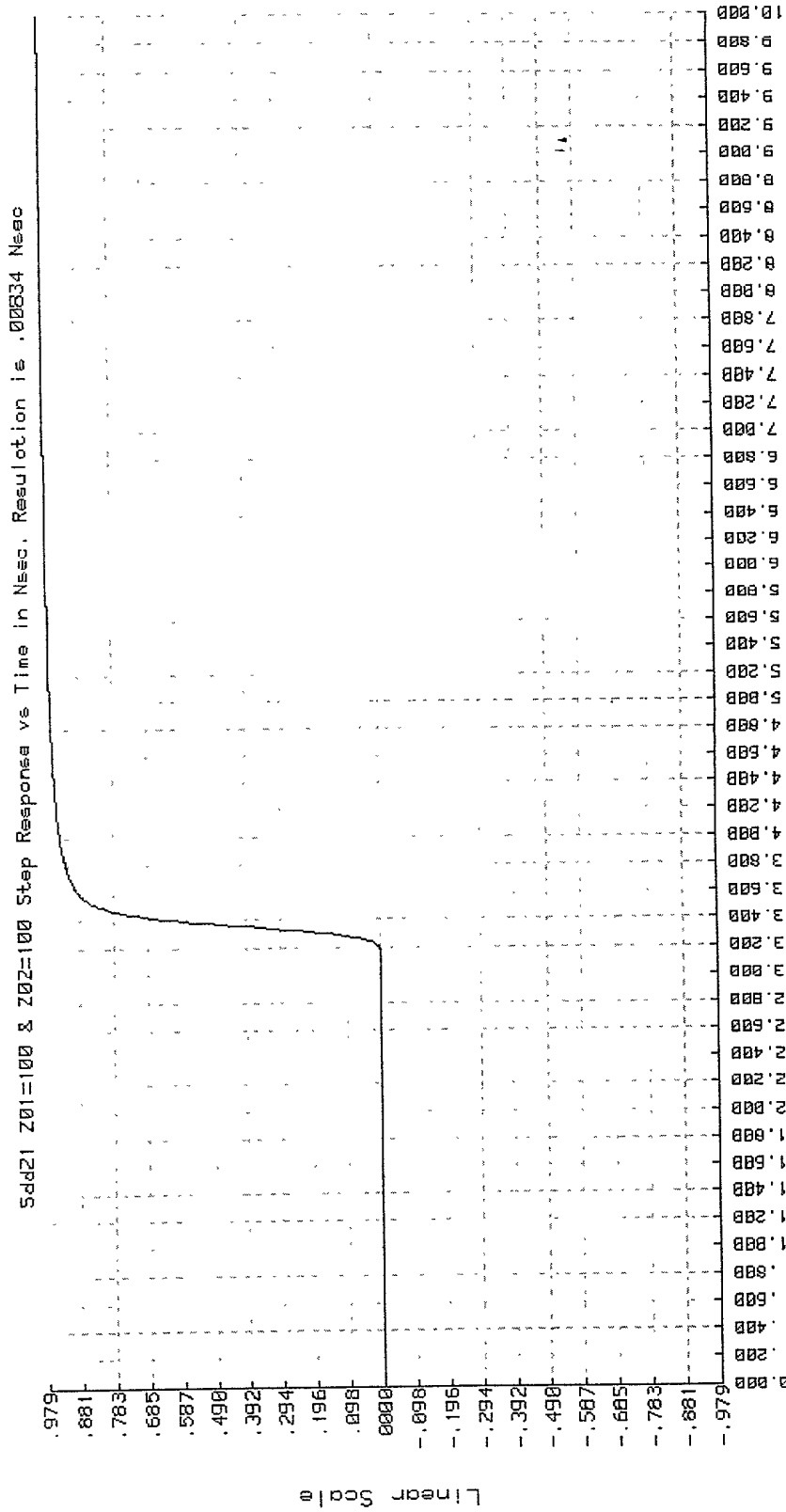


FIGURE 22

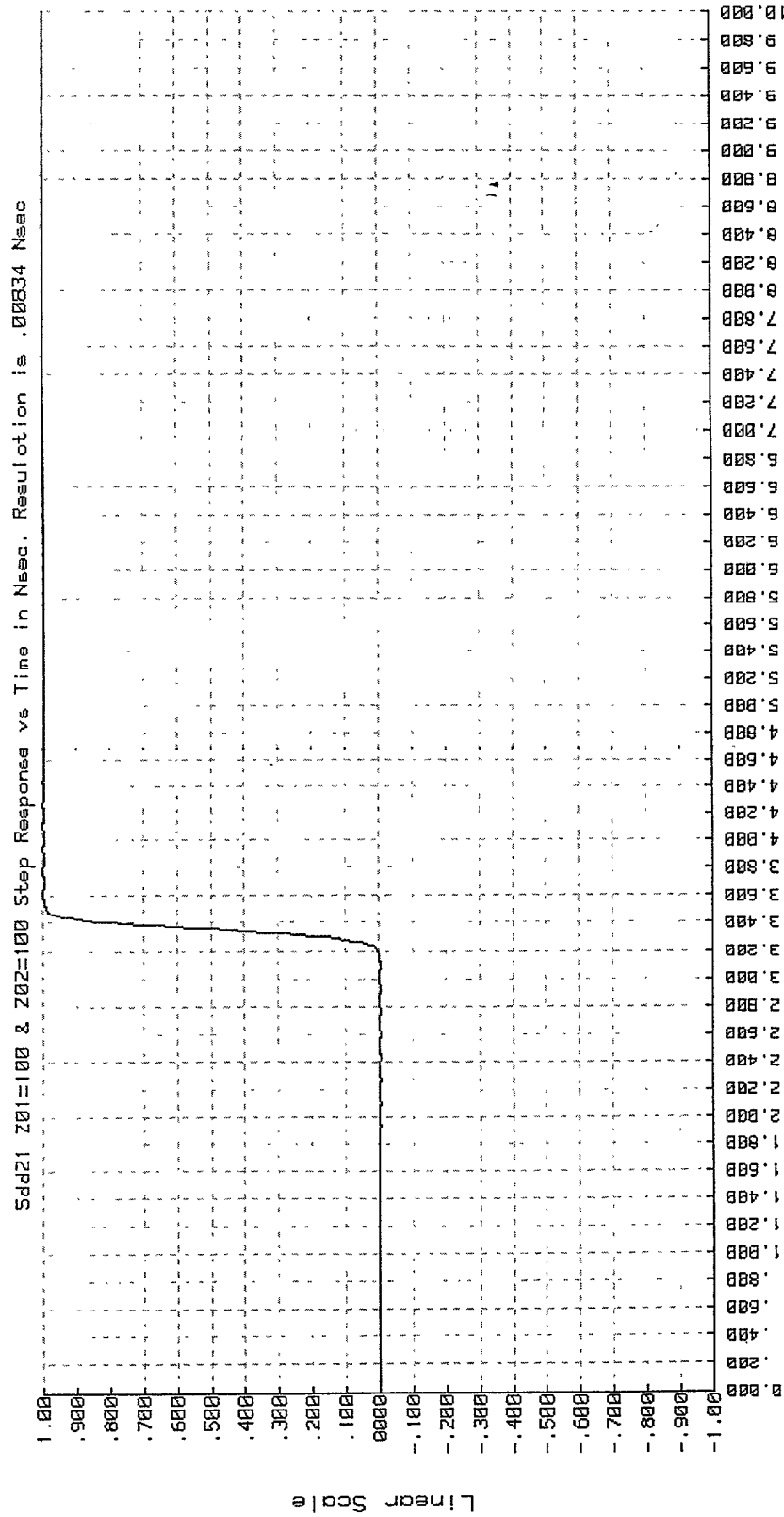
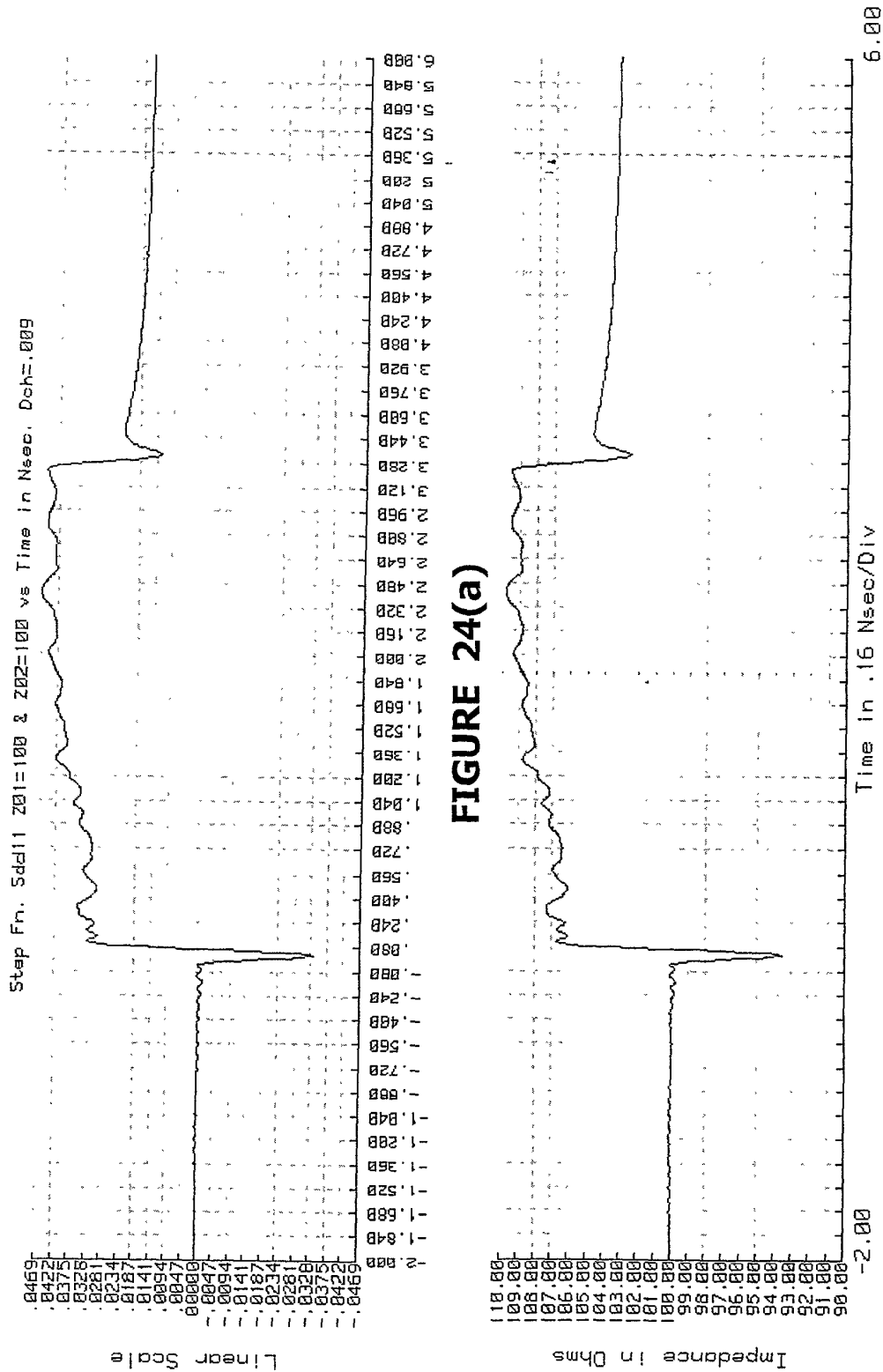


FIGURE 23



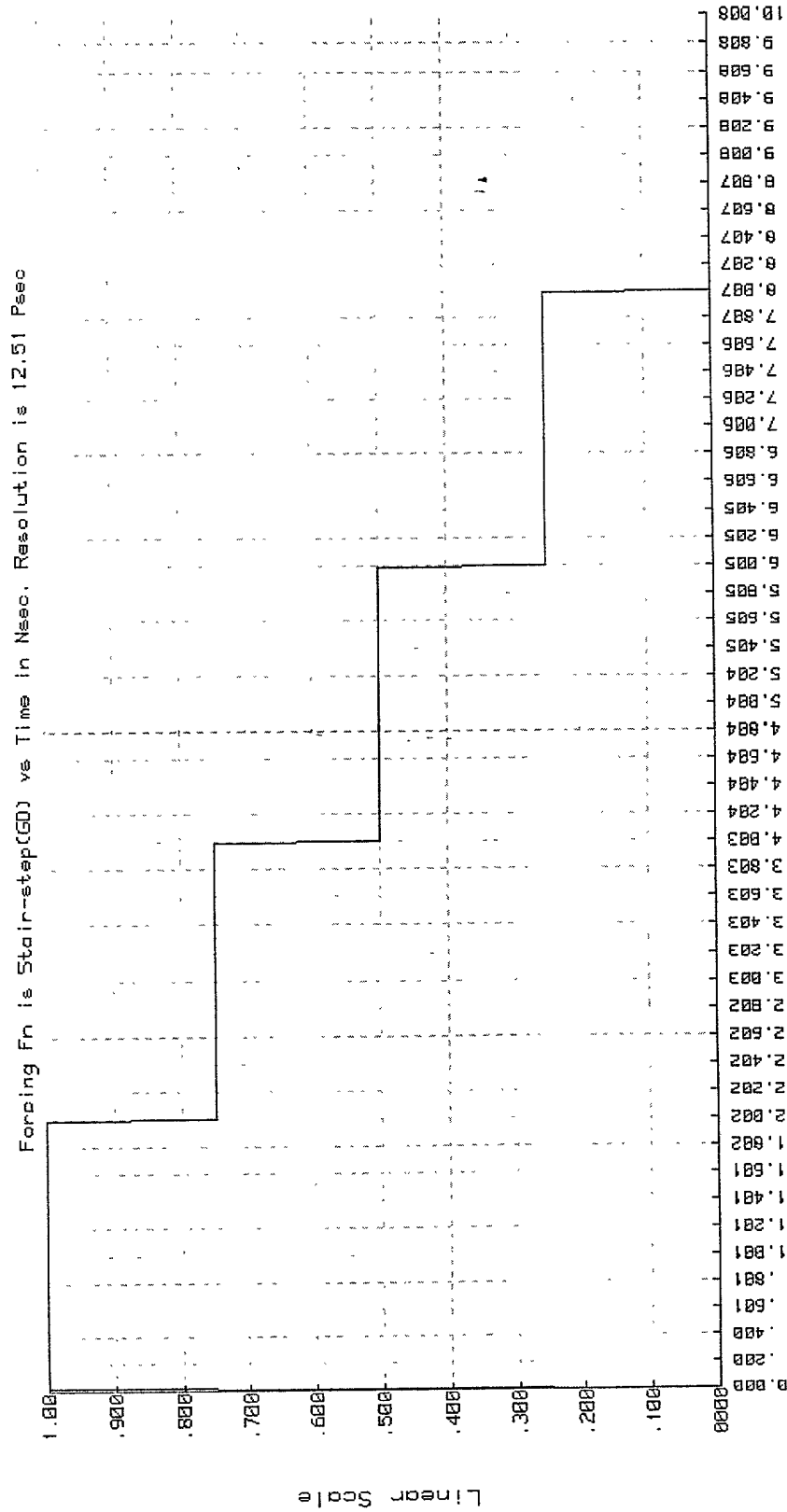


FIGURE 25

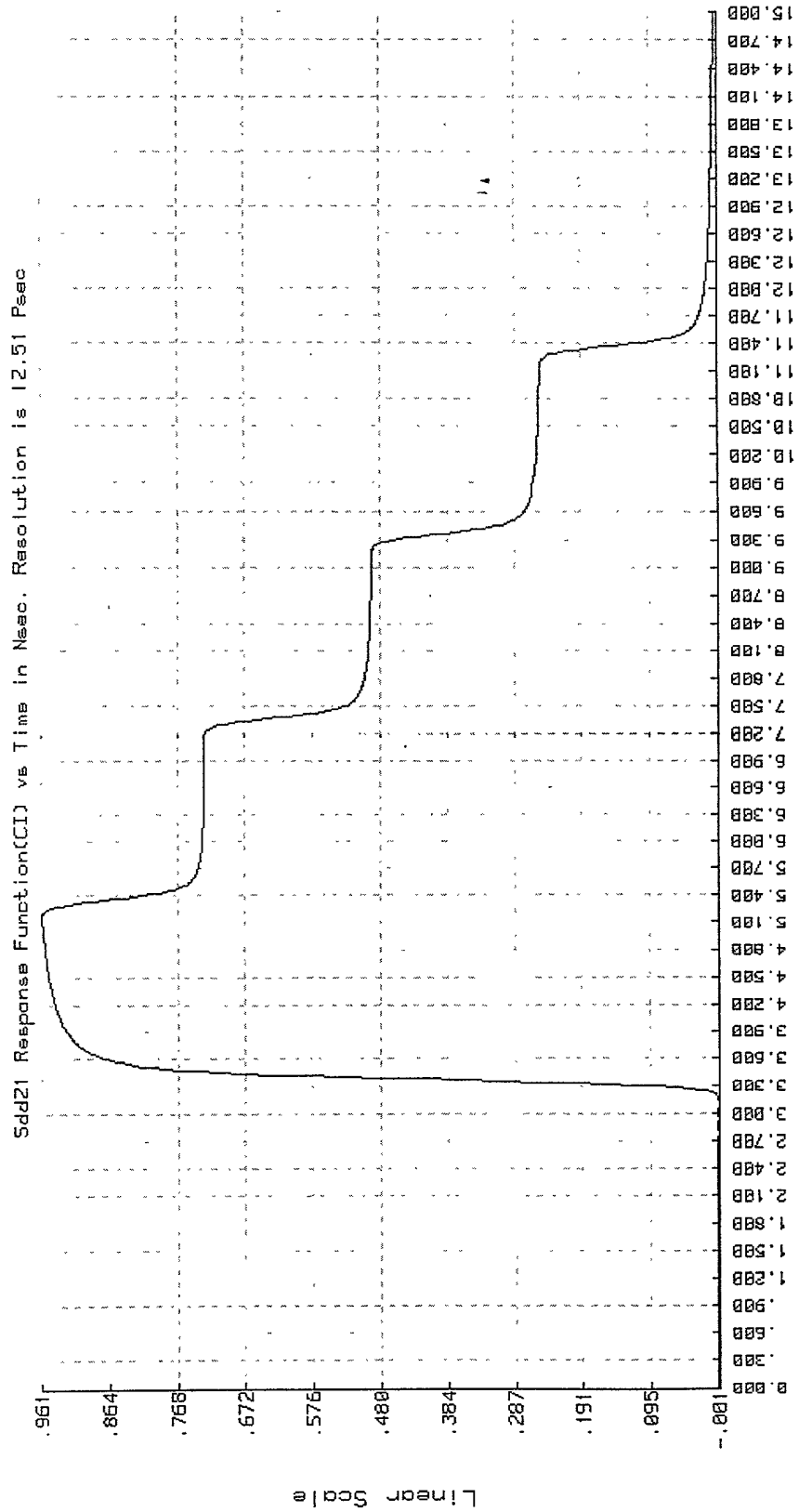


FIGURE 26

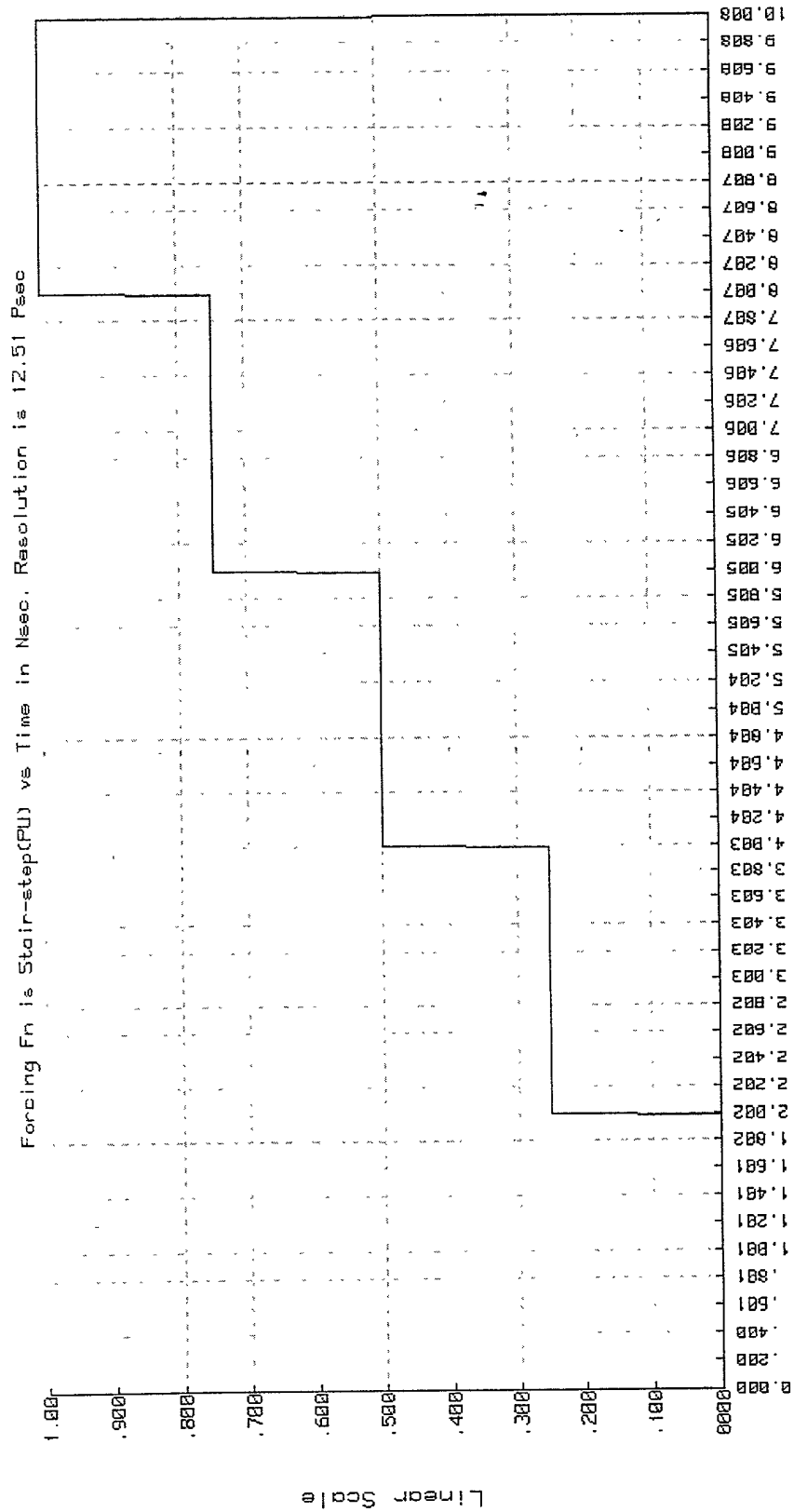


FIGURE 27

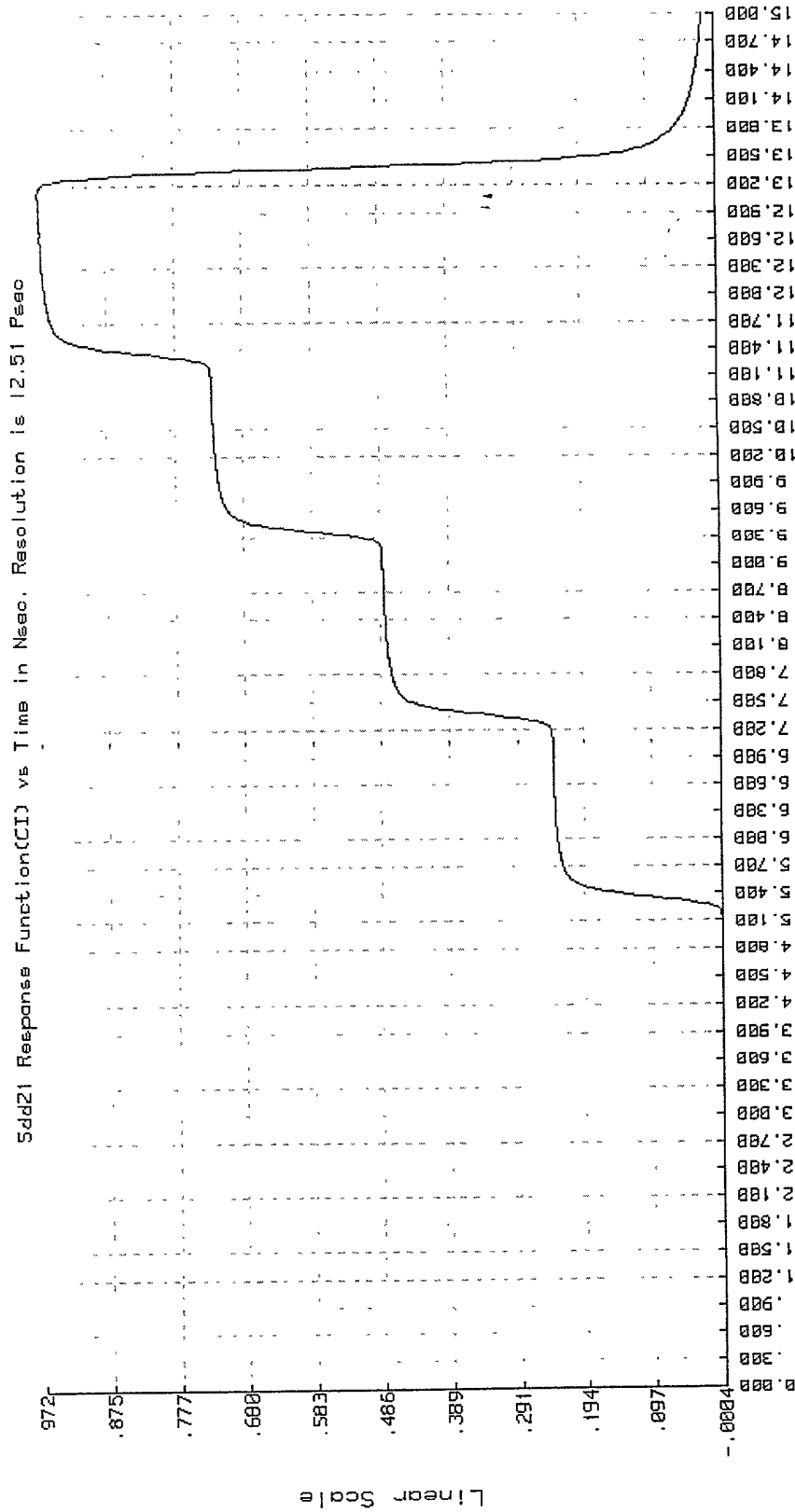


FIGURE 28



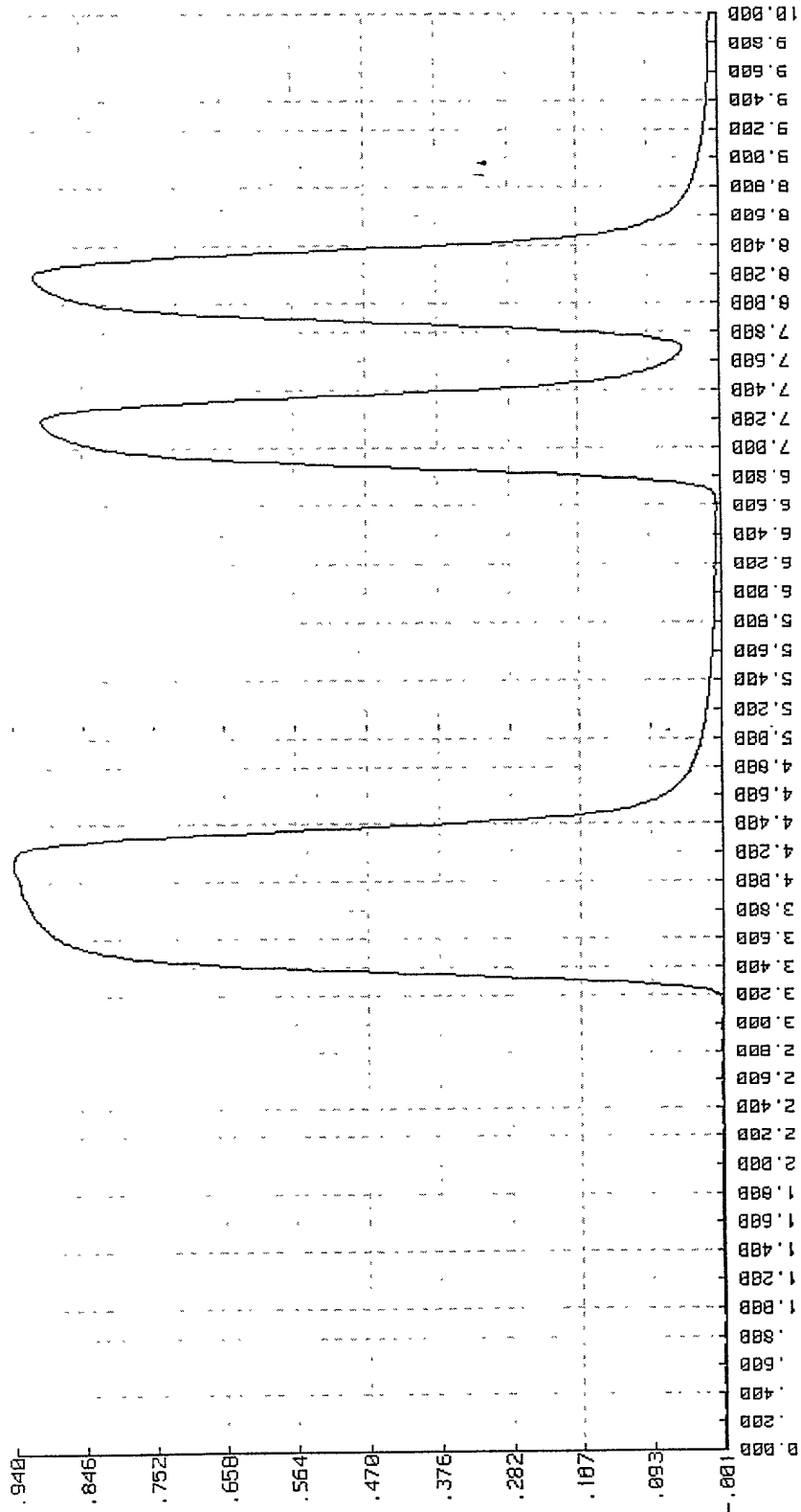


FIGURE 30

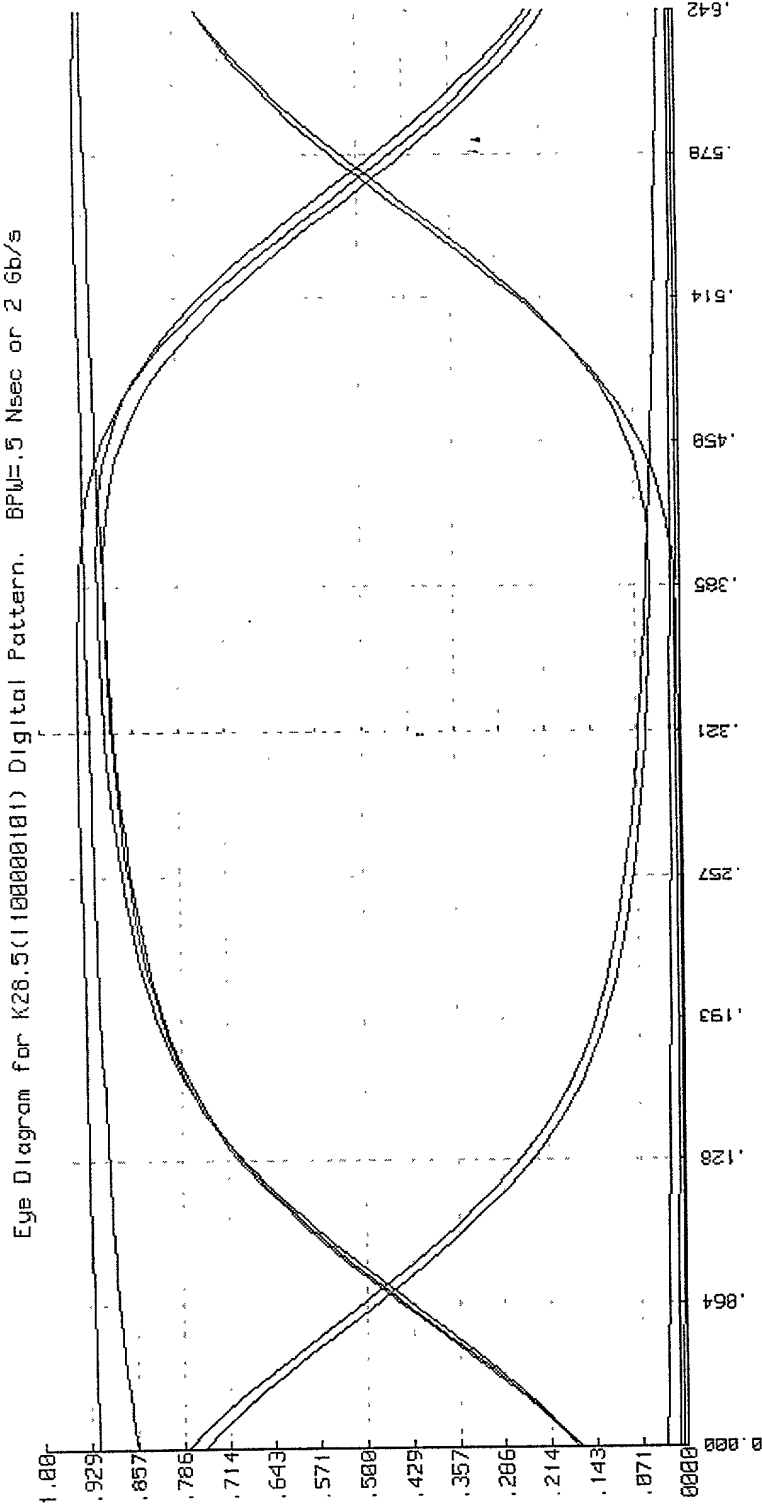


FIGURE 31

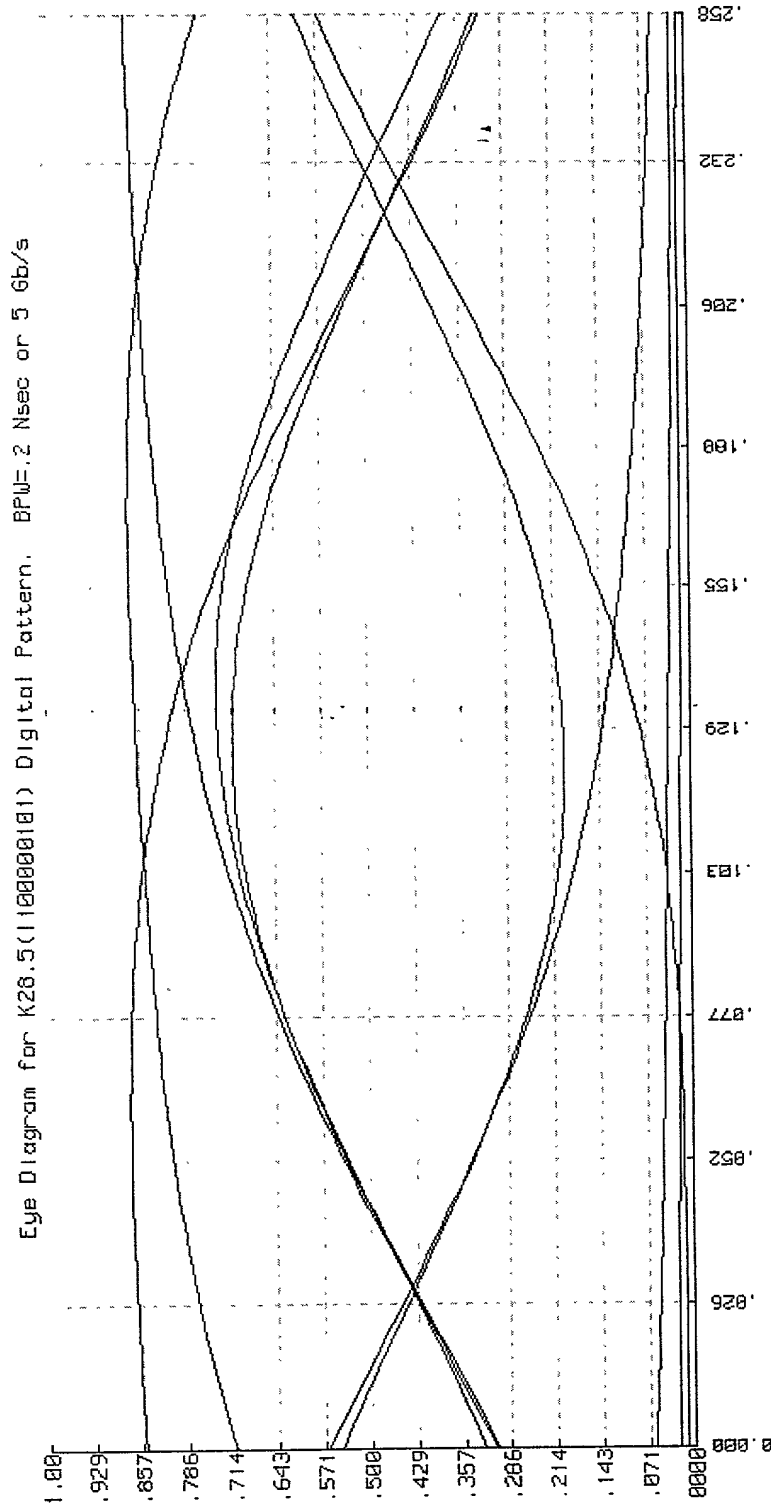


FIGURE 32

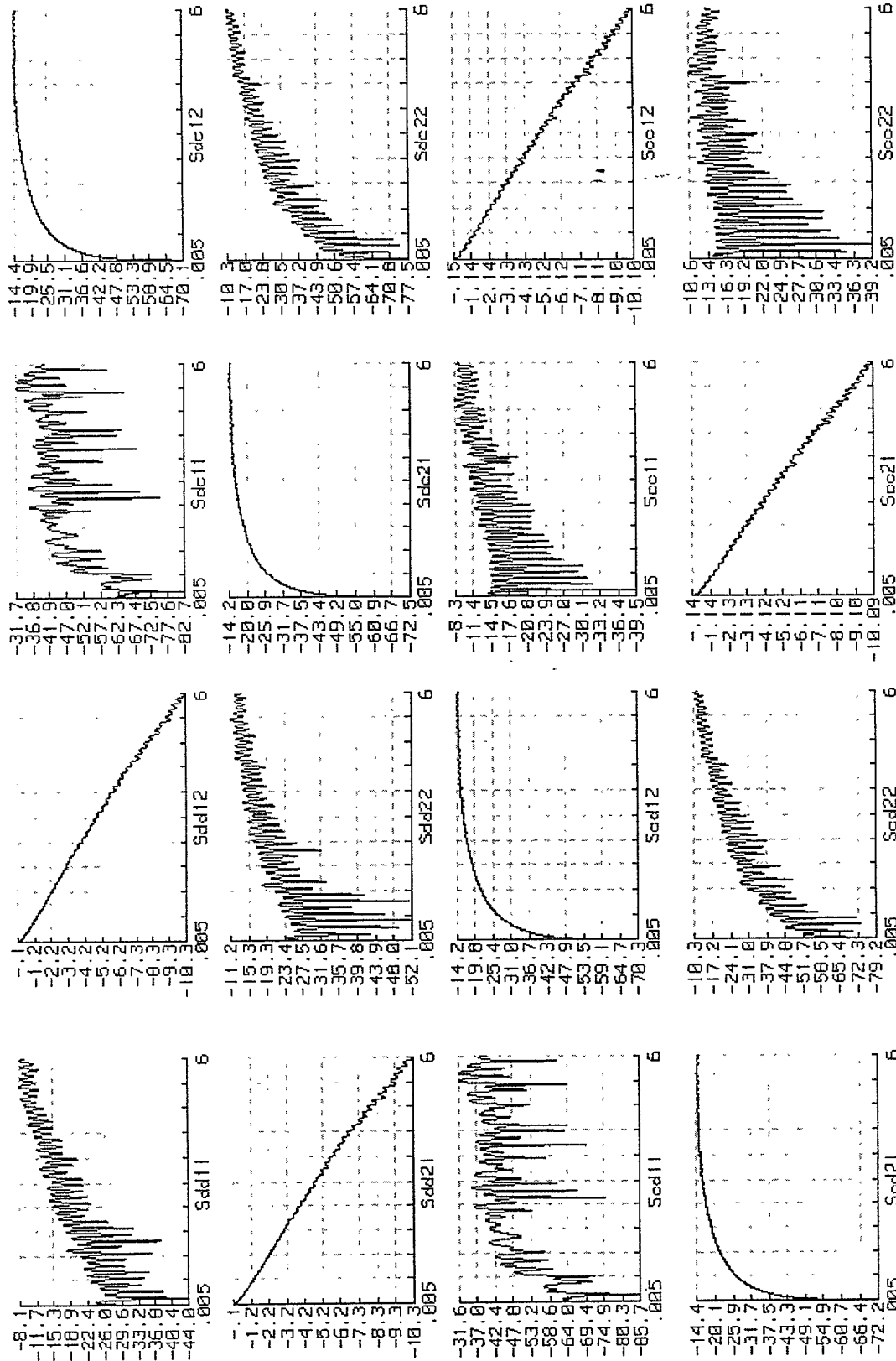


FIGURE 33

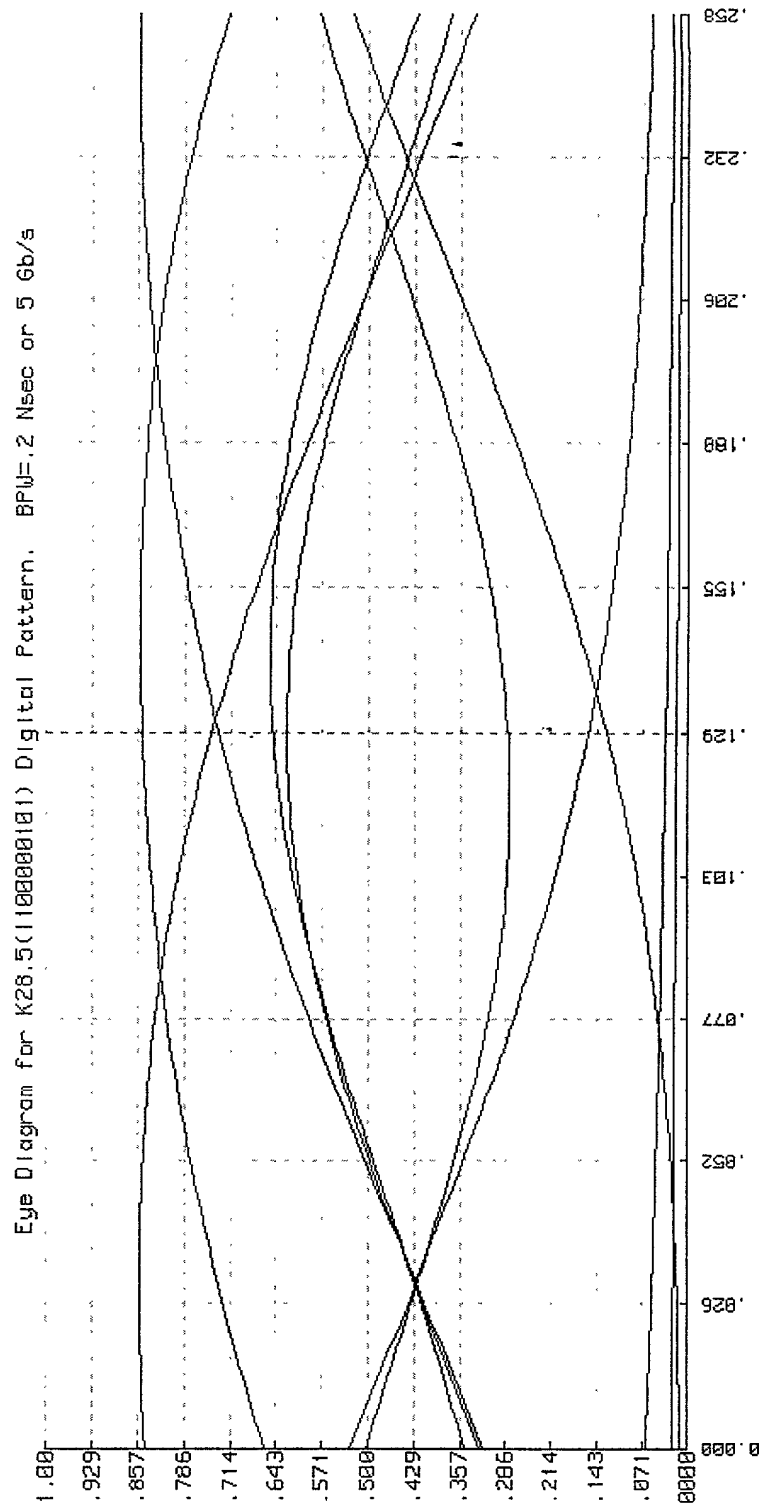


FIGURE 34